Electronic Version
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Claims

[c1] What is claimed is:

1.A method for fabricating a bit line contact hole, comprising:

providing a substrate having a main surface, on which at least two adjacent gate conductor stacks are provided, wherein a bit line contact area and a non-bit line contact area are defined over the main surface, wherein the bit line contact area is directly above an area between the two adjacent gate conductor stacks, and wherein each of the gate conductor stacks has a top surface and sidewalls;

depositing a silicon oxide liner on the top surface and sidewalls of each of the gate conductor stacks;

depositing a sacrificial layer on the silicon oxide liner;

performing a first chemical mechanical polishing (CMP) to polish the sacrificial layer to the top surface of the gate conductor stacks;

coating a spin-on-glass (SOG) layer onto the remaining sacrificial layer and onto the exposed top surface of the gate conductor stacks;

forming a photoresist pattern on the SOG layer masking the bit line contact area;

using the photoresist pattern as a hard mask, etching the SOG layer, the sacrificial layer, and the silicon oxide liner not covered by the photoresist pattern;
removing the photoresist pattern leaving the SOG layer, the sacrificial layer, and the silicon oxide liner within the bit line contact area intact;
depositing a silicon nitride liner on the SOG layer within the bit line contact area, the partial top surface and sidewalls of the gate conductor stacks;
depositing a dielectric layer over the silicon nitride liner;
performing a second CMP to polish the dielectric layer to stop on the SOG layer; and
selectively removing the remaining SOG layer and the sacrificial layer within the bit line contact area to form the bit line contact hole.

[c2] 2.The method according to claim 1 wherein the sacrificial polysilicon layer is made of polysilicon.

[c3] 3.The method according to claim 2 wherein the sacrificial layer is about 4000-angstrom thick.

[c4] 4.The method according to claim 1 wherein each of the gate conductor stacks comprises a gate dielectric layer, a conductive layer and a silicon nitride cap layer.

[c5] 5.The method according to claim 4 wherein the conduc-

tive layer comprises polysilicon.

[c6] 6.The method according to claim 4 wherein the conductive layer comprises metals.

[c7] 7.The method according to claim 1 wherein the dielectric layer is a borophosphosilicate glass (BPSG) layer.

[c8] 8.The method according to claim 1 wherein the SOG layer is about 3000-angstrom thick.